06-26-00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ruutu, et al.

Serial No. TO BE ASSIGNED

Corresponding to PCT/EP97/07264, filed 23 December 1997

Filed: 23 June 2000 Docket No.: 975.305USW1

Title: CLOCK GENERATING METHOD AND APPARATUS FOR AN ASYNCHRONOUS TRANSMISSION

CERTIFICATE UNDER 37 C.F.R. 1.10:
'Express Mail' mailing number: EL477365595US
Date of Deposit: 23 June 2000
The undersigned hereby certifies that this Transmittal Letter and the paper or fee, as described herein, are being deposited with the United States Postal Service 'Express Mail Post Office To Addressee' service under 37 CFR 1.10 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

By: Theresa Jurek
Theresa Jurek

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

REQUEST FOR CONTINUATION OF AN INTERNATIONAL APPLICATION UNDER 37 C.F.R. §1.53(b)

This is a request for filing a continuation application under 37 C.F.R. §1.53(b) of prior pending international application number PCT/EP97/07264 filed on 23 December 1997 entitled CLOCK GENERATING METHOD AND APPARATUS FOR AN ASYNCHRONOUS TRANSMISSION, which designated the United States.

1. ☒ Enclosed is a patent application containing 11 pages of specification, 3 pages of claims and 4 sheet(s) of drawings.

2. ☒ A preliminary amendment and Abstract page are enclosed.

3. ☒ Please amend the specification by inserting the following paragraph after the title:

   This application is a continuation of international application serial number PCT/EP97/07264, filed 23 December 1997.

4. ☐ Small entity status
   a. ☐ A small entity statement is enclosed.
   b. ☐ A small entity statement was filed in the prior non provisional application.
   c. ☐ is no longer claimed.

The filing fee is calculated below

CLAIMS				
	Number Filed	Number Extra	Rate	Fee
Total Claims	13	0	X $18.00	$
Indep. Claims	2	0	X $78.00	$
Multiply Dependent Claims				$
			Basic Fee	$ 690.00
			TOTAL	$ 690.00

5. ☒ Payment of filing fees
   - ☐ A check in the amount of is enclosed.
   - ☐ Please charge Deposit Account Number 50-1038.
   - ☒ Is deferred.

6. ☒ The Commissioner is hereby authorized to credit any overpayment or charge any fees required under 37 C.F.R. §1.16-1.18 to Deposit Account Number 50-1038.

7. ☐ The priority of application number , filed , is claimed under 35 U.S.C. §119.

8. ☒ An unsigned Declaration is enclosed.

9. ☐ An assignment of the invention to , Recordation Form Cover Sheet (Patents Only) and a check in the amount of $40.

10. ☐ An Information Disclosure Statement, Form PTO 1449 and copies of citations are enclosed.

11. ☒ Correspondence Address

Altera Law Group
10749 Bren Road East
Minneapolis, Minnesota 55343

12. ☒ Address all correspondence to Michael B. Lasky.

13. ☐ Also enclosed:

14. ☒ A return postcard is enclosed.

Respectfully submitted,

ALTERA LAW GROUP, LLC
10749 Bren Road East
Minneapolis, MN 55343-9056
(612) 912-0527

Dated: 23 June 2000

Michael B. Lasky
Atty. Reg. Number 29,555
MBL/mka

S/N UNKNOWN PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ruutu, et al.	Serial No.:	UNKNOWN
Filed:	CONCURRENT HEREWITH	Docket No.:	975.305USW1
Title:	CLOCK GENERATING METHOD AND APPARATUS FOR AN ASYNCHRONOUS TRANSMISSION		

CERTIFICATE UNDER 37 CFR 1.10
'Express Mail' mailing label number: EL477365595US
Date of Deposit: 23 June 2000
I hereby certify that this correspondence is being deposited with the United States Postal Service 'Express Mail Post Office To Addressee' service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C . 20231.

By: Theresa Jurek
Name: Theresa Jurek

PRELIMINARY AMENDMENT

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Please enter the following preliminary amendment into the above-referenced application.

ABSTRACT

Please insert the attached abstract into the application as the last page thereof.

CLAIMS

Please amend the claims as follows:

In claim 3, line 1, please remove “or 2”.

In claim 5, line 1, please replace “according to any one of the preceding claims” with –in claim 1--.

In claim 6, line 1, please replace “according to any one of the preceding claims” with –in claim 1--.

In claim 9, line 1, please remove "or 8".

In claim 11, line 1, please remove "or 10".

In claim 12, line 1, please replace "according to any one of claims 9 to 11" with –according to claim 9--.

In claim 13, line 1, please replace "according to any one of claims 7 to 12" with –according to claim 7--.

REMARKS

The above preliminary amendment is made to insert an abstract page into the application and to remove multiple dependencies from the following claims: 3, 5, 6, 9, 11, 12, and 13.

Applicant respectfully requests that this preliminary amendment be entered into the record prior to calculation of the filing fee and prior to examination and consideration of the above-identified application.

If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Applicant's attorney of record, Michael B. Lasky at (952) 912-0527.

Respectfully submitted,

ALTERA LAW GROUP, LLC
10749 Bren Road East
Minneapolis, MN 55343-9056
(612) 912-0527

Dated: 23 June 2000

Michael B. Lasky
Atty. Reg. Number 29,555
MBL/mka

ABSTRACT

CLOCK GENERATING METHOD AND APPARATUS FOR AN ASUNCHRONOUS TRANSMISSION

Clock generating method and apparatus for an asynchrouous transmission, wherein a plurality of actual receiving signal arrival times are detected and averaged, to thereby avoid influences of randomly distributed delay variations upon signal transmission. Clock synchronization between a transmitting clock and a receiving clock is recovered by correcting the receiving clock on the basis of the obtained average of the actual arrival times and an expected arrival time. Thereby, overflow and underflow of a receiver buffer can be prevented.

CLOCK GENERATING METHOD AND APPARATUS FOR AN ASYNCHRONOUS TRANSMISSION

FIELD OF THE INVENTION

The present invention relates to a method and apparatus for generating a clock for an asynchronous transmission, to be used especially in an ATM (Asynchronous Transfer Mode) connection between two devices of a Base Station Subsystem (BSS) in a GSM network.

BACKGROUND OF THE INVENTION

Usually, two elements of a Base Station Subsystem (BSS) in a GSM network are connected via a synchronous PCM connection. The principle of such an STM connection (Synchronous Transfer Mode) is shown in Fig. 1A. One of the devices, i.e. a transmitter 1, is selected as a master and its clock is used to synchronize PCM frames sent over the connection. The second device, i.e. a receiver 2, has a slave function, since its own clock is synchronized to the master clock of the transmitter.

In future ATM based GSM networks, a transcoder (TC) and a Base Transceiver Station (BTS) are connected via an asynchronous ATM connection, wherein synchronization is not available at the receiver 2. In an ATM connection, bit streams of binary signals of different channels are divided into unitary ATM cells to be transmitted in a time divisional manner. The cell rate defines the total number of ATM cells per second.

Fig. 1B shows the principle of such an ATM connection, wherein a transmitting clock generator 3 and a receiving

clock generator 4 are not synchronized and operate independently.

However, without a synchronization, the frequencies of the transmitting clock and the receiving clock are not equal. Therefore, a buffer of the receiver 2 may be filled gradually and a buffer overflow may occur, if the transmitting clock of the transmitter 1 is faster than the receiving clock of the receiver, since the buffer reading speed is slower than the writing speed. On the other hand, if the transmitting clock is slower than the receiving clock, the receiver 2 may run out of data (buffer underflow).

Both cases can result in lost data and, in case of time sensitive applications like GSM speech, cumulative delay that can rapidly become irritating. Thus, buffer underflow as well as buffer overflow is audible.

It is therefore an object of the present invention to provide a clock generating method and apparatus for an asynchronous transmission, by means of which clock synchronization between a transmitter and a receiver can be maintained.

This object is achieved by a clock generating method for an asynchronous transmission, comprising the steps of:

determining a plurality of actual signal arrival times;

averaging said plurality of actual signal arrival times; and

correcting a timing of a receiving clock on the basis of said average of the signal arrival times and an expected signal arrival time.

Furthermore, the above object is achieved by a clock generating apparatus for an asynchronous transmission, comprising:

determining means for determining an average of actual signal arrival times and for generating a control signal on the basis of said average of the actual signal arrival times and an expected signal arrival time; and

correcting means for correcting a timing of a receiving clock on the basis of said control signal.

Accordingly, since the timing of the receiving clock is corrected on the basis of an average of the actual arrival times of the signal and an expected arrival time, the receiving clock can be adjusted such that the expected arrival time coincides with the actual arrival time.

Moreover, by averaging the actual arrival time, delay variations upon signal transmission, which might cause synchronization errors, can be eliminated or at least significantly reduced.

Preferred developments of the present invention are defined in the subclaims.

BRIEF DESCRIPTION OF THE DRAWINGS

In the following, the invention and a preferred embodiment thereof will be described in greater detail with reference to the accompanying drawings in which:

Fig. 1A shows an STM transmission principle according to the prior art,

Fig. 1B shows an ATM transmission principle according to the prior art,

Fig. 2 shows a time chart for explaining an actual and an expected arrival time,

Fig. 3 shows a block diagram of a clock generating apparatus according to the preferred embodiment of the present invention,

Fig. 4 shows a flow diagram of a clock generating method according to the preferred embodiment of the present invention, and

Fig. 5 shows a block diagram of a determining means of the clock generating apparatus according to the preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The following preferred embodiment relates to an ATM connection between two devices of a Base Station Subsystem (BSS) in a GSM network as described above.

In the GSM network, a full rate TRAU (Transcoder and Rate Adaption Unit) frame is packed inside one ATM cell. The TRAU frame is an information packet transferred between the TC and the BTS and may contain 20 ms of coded speech. Thus, the ATM cells are transmitted with an intervall of 20 ms corresponding to a cell rate r = 50 cells/s. The clock frequencies f_t, f_r of the transmitter 1 and the receiver 2

can be obtained from the cell rate r using $f_{t,r} = R \cdot r$, wherein R denotes the ratio between the clock frequency and the cell rate. For simplicity, it is assumed in the following that the clock frequencies f_t, f_r of the transmitter 1 and the receiver 2 are equal to the cell rate (R=1).

Fig. 2 shows an example for actual arrival times t_{i-1} and t_i of two adjacent cells i-1 and i at the receiver 2. According to the clock of the receiver 2, the cell i is expected to arrive after an interval Δt_r. However, due to a difference in the clock frequencies of the transmitter 1 and receiver 2, the cell i actually arrives after an interval Δt_t shorter than the expected interval Δt_r. Thus, in the present case, the clock frequency f_t of the transmitter 1 is higher than the clock frequency f_r of the receiver 2.

Accordingly, from the viewpoint of the receiver 2, the transmitter 1 is transmitting at a cell rate higher than 50 cells/s.

On the other hand, the clock frequency f_t of the transmitter 1 may be lower than the clock frequency f_r of the receiver 2. In this case, the interval Δt_t is longer than the expected interval Δt_r and, from the viewpoint of the receiver 2, the transmitter 1 is transmitting at a cell rate lower than 50 cells/s.

In order to recover synchronization, the clock frequency f_r of the receiver 2 has to be corrected so as to be equal to the clock frequency f_t of the transmitter 1. Thus:

$$f_r^{corr} = f_t = \frac{1}{\Delta t_t} \quad (1)$$

The correction can be performed on the basis of the difference Δf between the clock frequencies f_t and f_r, which can be obtained as follows:

$$\Delta f = f_t - f_r = \frac{1}{\Delta t_t} - \frac{1}{\Delta t_r} = \frac{\Delta t_r - \Delta t_t}{\Delta t_t \Delta t_r} = \frac{C - \Delta t_t}{\Delta t_t C} \quad (2)$$

wherein the constant C represents the time interval Δt_r which is fixed from the viewpoint of the receiver 2, assuming that the frequency f_r of the receiving clock does not vary. It is to be noted that Δf may also be a negative, if $f_t < f_r$.

As already mentioned, according to the GSM specifications, the cell rate is 20 ms during normal speech transmission. Thus, the constant C is set to 20 ms. In case of Discontinuous Transmission (DTX), only TRAU frames containing a comfort noise information are sent every 480 ms, which means that, in this case, C has to be set to 480 ms.

In order to perform correction, the above frequency difference Δf has to be added to the frequency f_r of the receiving clock of the receiver 2, so that the receiver 2 operates substantially at the same frequency as the transmitter 1. Thus, the corrected clock frequency f_r^{corr} of the receiver 2 can be obtained as follows:

$$f_r^{corr} = f_r + \frac{C - \Delta t_t}{\Delta t_t C} \qquad (3)$$

Here, it is assumed that the difference between the time intervals Δt_r and Δt_t only results from a clock difference between the transmitter 1 and the receiver 2.

However, the above time difference between the actual and expected arrival times is not only caused by the difference between the clock frequencies f_r and f_t but also by a signal delay due to the signal propagation via the ATM network. Namely, an ATM cell carrying a TRAU frame has a so-called time-dependent Cell Delay Variation (CDV) caused by the ATM network.

Thus, the time interval Δt_t actually results from the sum of the instantaneous CDV and the clock period of the transmitter, and can be obtained as follows:

$$\Delta t_t = \Delta t_{CDV}^i + \frac{1}{f_t} \qquad (4)$$

wherein the index i denotes an ith cell.

However, if the actual arrival time is largely affected by the CDV, the receiving clock is mainly adjusted to the more or less random CDV and not to the transmitting clock. Nevertheless, in view of the fact that the CDV is randomly distributed with a mean value of zero, the CDV can be eliminated by obtaining an average Δt_t^{ave} over a certain number N of samples.

By replacing Δt_t by Δt_t^{ave} in equation (3), a good estimation of the actually required corrected frequency of the receiving clock can be obtained as follows:

$$f_r^{corr} = f_r + \frac{C - \Delta t_t^{ave}}{\Delta t_t^{ave} C} \qquad (5)$$

The average value Δt_t^{ave} is calculated as follows:

$$\Delta t_t^{ave} = \frac{1}{N}\sum_{i=1}^{N} \Delta t_{CDV}^{i} + \frac{1}{N}\sum_{i=1}^{N} \frac{1}{f_t}, \qquad (6)$$

wherein N should be selected such that the first sum of equation (6) can be neglected.

The practical value of N depends on the magnitude of the CDV and the desired accuracy and may be in a range between 100 and 10^5. In the present speech channel, N=100 corresponds to 2 seconds of speech. Thus, a practical value could be $N=10^4$ corresponding to 3 min of speech, which can be achieved during a telephone call. If the present invention is applied to transmission with higher bit rates, N can be chosen even larger.

During the Discontinuous Transmission (DTX), where C=480 ms, N could be incremented by one every 20ms or by 24 every 480ms during the calculation of the above sums.

However, if N is too small, the resulting difference between the actual and the expected arrival time of the cells may even increase due to the random distribution of the CDV.

Fig. 3 shows a block diagram of the preferred embodiment. The receiving clock of the receiver 2 is corrected by means of a voltage controlled oscillator (VCO) 40 or any other controllable signal generator. A control signal supplied to the VCO 40 is derived from the output of a determining means 20 to which the actual receiving clock and the receiving signal, i.e. ATM cells, are supplied and which generates an output signal according to the above equation (5).

The output signal of the determining means 20 can be supplied to the VCO 40 via an integrator 30 so as to improve accuracy and stability of correction.

Fig. 4 illustrates a flow chart of the signal processing steps performed in the determining means 20.

At first, in step 100, a counting variable i is set to 0 and a timer implemented by hardware or software is started when the first ATM cell is received. Subsequently, the timer is stopped when the next ATM cell is received to thereby obtain the value of Δt_t as a result of counting (step 101). The obtained value of Δt_t is stored (step 102) and the timer is reset and started again when a new cell is received, wherein the value i is incremented (step 103).

In step 104, it is determined whether i has reached the value N, i.e. whether N samples have been stored. If so, the average value Δt_t^{ave} is calculated in step 105 by adding the

stored values of Δt_t and deviding the sum by N. In case i is smaller than N, the flow returns to step 101 in order to repeat steps 101 to 104 until i equals N.

After the average value Δt_t^{ave} has been calculated, the correction value for the frequency f_r of the receiving clock is calculated in accordance with equation (5). The obtained correction value is used to control the VCO 40 or any other clock generation means.

The determining means 20 may be constituted as shown in Fig. 5. A detecting means 21 is provided for detecting the actual arrival time of ATM cells. In accordance with the above described steps, the detecting means may comprise a timer. The obtained values of Δt_t are stored in a storing means 22 in order to be used by an averaging means 23 in order to obtain an average over N sample values. The obtained average of the actual arrival times is supplied to a correction control means 24 together with the receiving clock. The correction control means 24 generates a control signal in accordance with the above equation (5). Thus, it essentially works as a time difference calculator.

The above described detecting means 20 according to Fig. 5 may be implemented by discrete hardware components or by a CPU which is controlled on the basis of a control program.

In case of a hardware implementation, the correction control means 24 may comprise a phase detector which may operate as follows.

If the time difference is positive, i.e. the actual arrival time is shorter than the expected arrival time ($\Delta t_t < \Delta t_r$), a pulse of a first polarity (e.g. positive pulse) is generated as the control signal, and if the result is negative, i.e. $\Delta t_t > \Delta t_r$, a pulse of a second polarity (e.g. negative polarity) is generated. These pulses are used to control the VCO 40. Thus, only a comparison between the time intervals Δt_t and Δt_r is actually required in order to correct the clock frequency of the receiver 2.

In summary, a clock generating method and apparatus for an asynchronous transmission are disclosed, wherein a plurality of actual receiving signal arrival times are detected and averaged, to thereby avoid influences of randomly distributed delay variations upon signal transmission. Clock synchronization between a transmitting clock and a receiving clock is obtained by correcting the receiving clock on the basis of the obtained average of the actual arrival times and an expected arrival time. Thereby, overflow and underflow of a receiver buffer can be prevented.

It should be understood that the above description and accompanying figures are only intended to illustrate the present invention. Thus, the method and apparatus according to the invention may also be used in systems other than the described GSM system. The preferred embodiment of the invention may thus vary within the scope of the attached claims.

Claims:

1. A clock generating method for an asynchronous transmission, comprising the steps of:

determining a plurality of actual signal arrival times;

averaging said plurality of actual signal arrival times; and

correcting a timing of a receiving clock on the basis of said average of the signal arrival times and an expected signal arrival time.

2. A method according to claim 1,

wherein said expected signal arrival time is derived from said receiving clock.

3. A method according to claims 1 or 2,

wherein said determining step comprises counting a time period between the arrival of a first and the arrival of a subsequent second signal.

4. A method according to claim 3,

wherein said averaging step comprises storing said counted time periods and calculating an average of said stored time periods.

5. A method according to any one of the preceding claims, wherein said correcting step comprises determining a difference between a frequency corresponding to said average of said plurality of actual signal arrival times and a frequency of said receiving clock, and changing the frequency of said receiving clock according to said frequency difference.

6. A method according to any one of the preceding claims, wherein the asynchronous transmission is an ATM transmission and the signal is an ATM cell.

7. A clock generating apparatus for an asynchronous transmission, comprising:

determining means **(20)** for determining an average of actual signal arrival times and for generating a control signal on the basis of said determined average of the actual signal arrival times and an expected signal arrival time; and

correcting means **(40)** for correcting a timing of a receiving clock on the basis of said control signal.

8. An apparatus according to claim 7,

wherein said correcting means comprises a voltage controlled oscillator **(40)**.

9. An apparatus according to claims 7 or 8,

wherein said determining means **(20)** comprises:

detecting means (21) for detecting an actual arrival time of a signal;

averaging means (23) for averaging a plurality of detected actual signal arrival times in order to obtain said average of the actual signal arrival times; and

correction control means (24) for comparing said average of the actual signal arrival times with said expected signal arrival time and for generating said control signal in accordance with the comparison result, wherein said expected signal arrival time is derived from said receiving clock.

10. An apparatus according to claim 9,

wherein said determining means (20) comprises storing means (22) for storing said plurality of detected actual signal arrival times.

11. An apparatus according to claims 9 or 10,

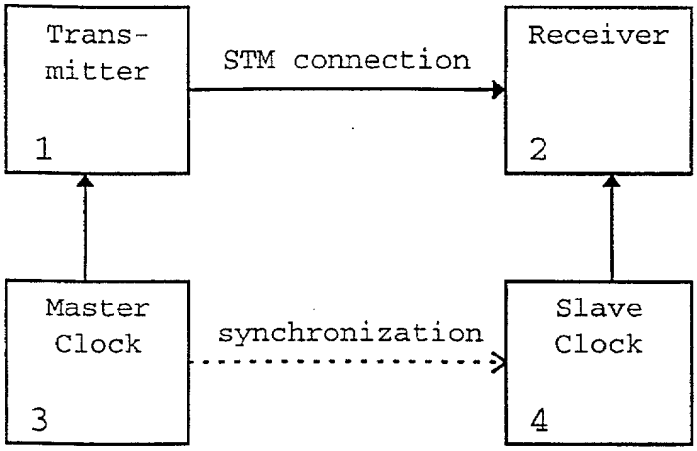
wherein said detecting means (20) comprises timer.

12. An apparatus according to any one of claims 9 to 11,

wherein said correction control means (24) comprises a phase detector, and wherein a polarity of said control signal is changed in accordance with the result of comparison.

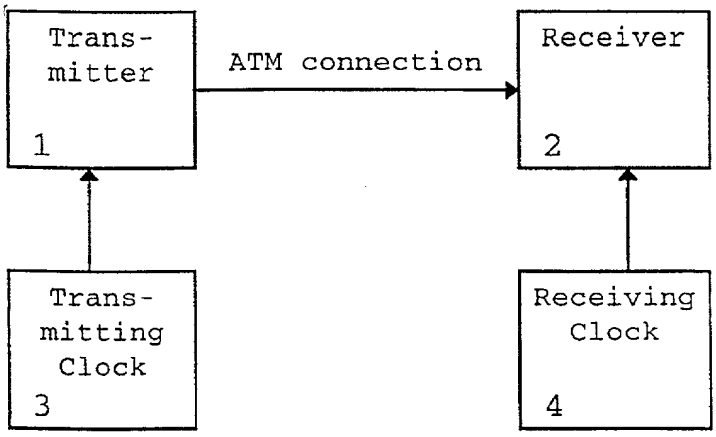
13. An apparatus according to any one of claims 7 to 12,

wherein the asynchronous transmission is an ATM transmission and the signal is an ATM cell.



PRIOR ART

Fig. 1A



PRIOR ART

Fig. 1B

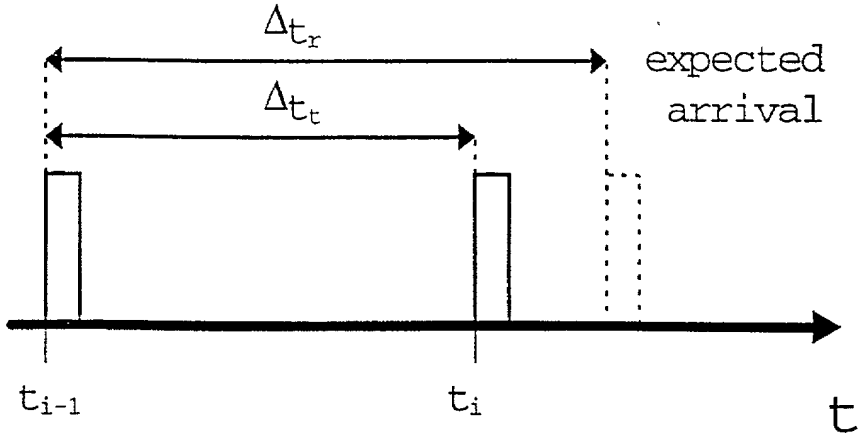

Δt_r
Δt_t
expected
arrival
t_{i-1}
t_i
t

Fig. 2

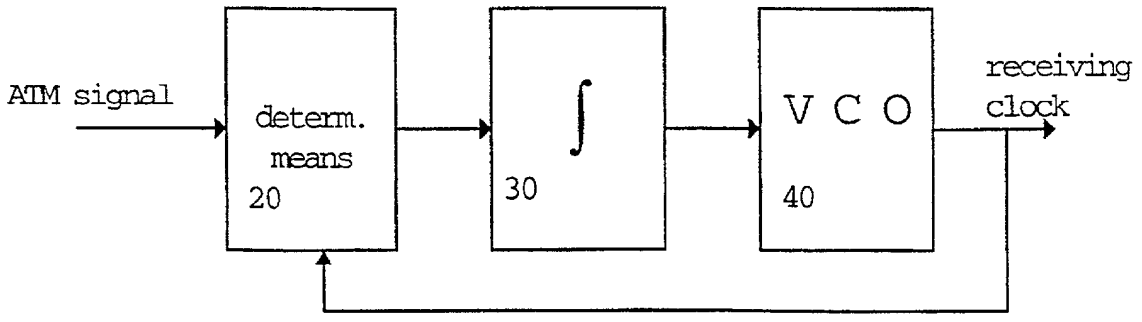

ATM signal
determ.
means
20
∫
30
V C O
40
receiving
clock

Fig. 3

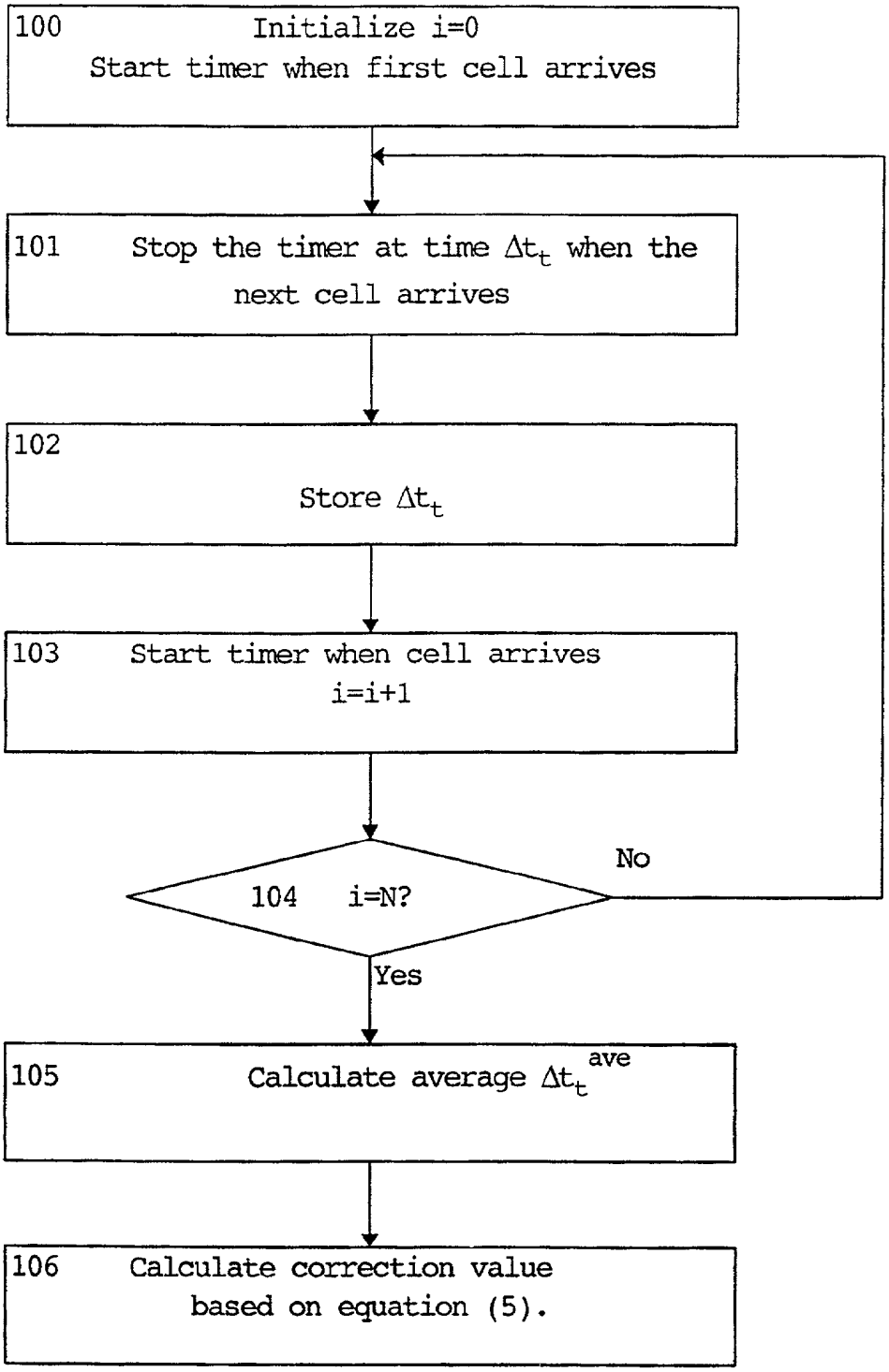

100 Initialize i=0
Start timer when first cell arrives
101 Stop the timer at time Δt_t when the next cell arrives
102 Store Δt_t
103 Start timer when cell arrives
i=i+1
104 i=N?
No
Yes
105 Calculate average Δt_t^{ave}
106 Calculate correction value based on equation (5).

Fig. 4

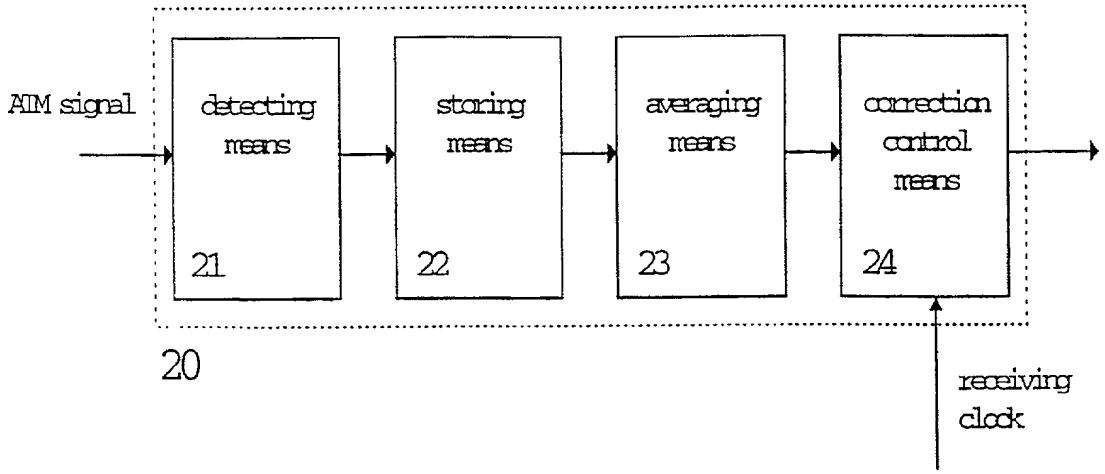

AIM signal
detecting means
21
storing means
22
averaging means
23
correction control means
24
20
receiving clock

Fig. 5

Altera Reference No.: 975.305USW1

Altera Law Group, LLC

Declaration and Power of Attorney Patent Application (Design or Utility)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: CLOCK GENERATING METHOD AND APPARATUS FOR AN ASYNCHRONOUS TRANSMISSION

the specification of which

- ☐ is referred to by Altera reference number on a separate document
- ☒ is attached hereto
- ☐ was filed on 23 June 2000 as application serial no. _____ and or PCT International Application number and was amended on (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information know to me to be material to patentability as defined in 37 C.F.R.§1.56.

I hereby claim foreign priority benefits under 35 U.S.C.§119(a)-(d) or 35 U.S.C.§365(b) of any foreign application(s) for patent or inventor's certificate, or 35 U.S.C.§365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate of PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)		
Number	**Country**	**Day/Month/Year Filed**
Number	**Country**	**Day/Month/Year Filed**
Number	**Country**	**Day/Month/Year Filed**

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below:

Prior Provisional Application(s)	
Serial Number	**Day/Month/Year Filing Date**
Serial Number	**Day/Month/Year Filing Date**
Serial Number	**Day/Month/Year Filing Date**

I hereby claim the benefit under 35 U.S.C. §120 of any United States application(s), or under 35 U.S.C. §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. §112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in 37 C.F.R.§1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

Prior U.S. or International Application(s)		
Serial Number PCT/EP97/07264	**Day/Month/Year Filed** 23 December 1997	**Status** (patented, pending, abandoned) Pending
Serial Number	**Day/Month/Year Filed**	**Status** (patented, pending, abandoned)
Serial Number	**Day/Month/Year Filed**	**Status** (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C.§1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Altera Reference No.: 975.305USW1

Power of Attorney

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Steven R. Funk	Reg. No. 37,830	Mark A. Hollingsworth	Reg. No. 38,491
David W. Lynch	Reg. No. 36,204	Michael B. Lasky	Reg. No. 29,555
Karen D. McDaniel	Reg. No. 37,674	Iain A. McIntyre	Reg. No. 40,337

I hereby authorize them or others whom they may appoint to act and rely on instructions from and communicate directly with the person/organization who/which first sends this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Altera Law Group, LLC otherwise.

Please direct all correspondence in this case to Altera Law Group, LLC at the address indicated below:

Michael B. Lasky
Altera Law Group, LLC
10749 Bren Road East, Opus 2
Minneapolis, MN 55343

Full Name of Sole or First Inventor		
Family Name Ruutu	**First Given Name** Jussi	**Second Given Name**
Residence and Citizenship		
City of Residence Helsinki	**State or Country of Residence** Finland	**Country of Citizenship** Finland
Post Office Address		
Street Address Nokia Research Center P.O. Box 45	**City** FIN-00211 Helsinki	**State & Zip Code or Country** FINLAND
Signature of Inventor		**Date**

Full Name of Second Inventor, if any		
Family Name Kaaresoja	**First Given Name** Topi	**Second Given Name**
Residence and Citizenship		
City of Residence Helsinki	**State or Country of Residence** Finland	**Country of Citizenship** Finland
Post Office Address		
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